WHAT IS CLAIMED IS:

1. An electric characteristic evaluating apparatus for extracting electric characteristics of a semiconductor device by numerically solving physical equations describing physical phenomenon in a semiconductor device comprising:

an integral value calculator configured to integrate a carrier generation and extinction speed obtained by numerically solving the physical equations, in each carrier generation and extinction mechanism within a semiconductor region, and issue the result obtained by integration respectively.

2. The electric characteristic evaluating apparatus according to claim 1, wherein the volume integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-3} time^{-1}, the surface integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-2} time^{-1}, and the line integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-1} time^{-1}.

3. The electric characteristic evaluating apparatus according to claim 1, wherein the carrier generation and extinction mechanism includes a SRH process, impact ionization, and inter-band tunneling.

4. The electric characteristic evaluating apparatus according to claim 1, wherein said integral value calculator issues an output by multiplying a charge amount to each integral value of each carrier generation and extinction mechanism.

5. The electric characteristic evaluating apparatus according to claim 1, wherein the electric characteristics

are extracted repeatedly varying a bias condition to the semiconductor device.

6. An electric characteristic evaluating method for extracting electric characteristics of a semiconductor device by numerically solving physical equations describing physical phenomenon in a semiconductor device comprising the steps of:

integrating a carrier generation and extinction speed obtained by numerically solving the physical equations, in each carrier generation and extinction mechanism within a semiconductor region; and

issuing the result obtained by integration respectively.

7. The electric characteristic evaluating method according to claim 6, wherein the volume integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-3} time^{-1}, the surface integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-2} time^{-1}, and the line integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-1} time^{-1}.

8. The electric characteristic evaluating method according to claim 6, wherein the carrier generation and extinction mechanism includes a SRH process, impact ionization, and inter-band tunneling.

9. The electric characteristic evaluating method according to claim 6, wherein an output is issued by multiplying a charge amount to each integral value of each carrier generation and extinction mechanism.

10. The electric characteristic evaluating method

according to claim 6, wherein the electric characteristics are extracted repeatedly varying a bias condition to the semiconductor device.

11. An electric characteristic evaluating program for extracting electric characteristics of a semiconductor device by numerically solving physical equations describing physical phenomenon in a semiconductor device comprising and making a computer system execute the process of:

an integral value calculating process of integrating a carrier generation and extinction speed obtained by numerically solving the physical equations, in each carrier generation and extinction mechanism within a semiconductor region, and issuing the result obtained by integration respectively.

12. The electric characteristic evaluating program according to claim 11, wherein the volume integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-3} time^{-1}, the surface integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-2} time^{-1}, and the line integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-1} time^{-1}.

13. The electric characteristic evaluating program according to claim 11, wherein the carrier generation and extinction mechanism includes a SRH process, impact ionization, and inter-band tunneling.

14. The electric characteristic evaluating program according to claim 11, wherein an output is issued by multiplying a charge amount to each integral value of each carrier generation and extinction mechanism.

15. The electric characteristic evaluating program according to claim 11, wherein the electric characteristics are extracted repeatedly varying the bias condition to the semiconductor device.

16. A semiconductor device manufacturing method for extracting electric characteristics of a semiconductor device by numerically solving physical equations describing physical phenomenon in a semiconductor device, determining the manufacturing condition of semiconductor device from the extracted electric characteristics, and manufacturing the semiconductor device on the basis of the determined manufacturing condition comprising the steps of:

integrating a carrier generation and extinction speed obtained by numerically solving the physical equations, in each carrier generation and extinction mechanism within a semiconductor region, and issuing the result obtained by integration respectively; and

determining the manufacturing condition of the semiconductor device having the desired electric characteristics on the basis of the result obtained by integration.

17. The semiconductor device manufacturing method according to claim 16, wherein the volume integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-3} time^{-1}, the surface integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-2} time^{-1}, and the line integration is effected on the carrier generation and extinction mechanism having the dimension of length^{-1} time^{-1}.

18. The semiconductor device manufacturing method

according to claim 16, wherein the carrier generation and extinction mechanism includes a SRH process, impact ionization, and inter-band tunneling.

19. The semiconductor device manufacturing method according to claim 16, wherein an output is issued by multiplying a charge amount to each integral value of each carrier generation and extinction mechanism.

20. The semiconductor device manufacturing method according to claim 16, wherein the electric characteristics are extracted repeatedly varying a bias condition to the semiconductor device.